The invention is claimed as follows:

1. A semi-conductor substrate package comprising;

a substrate;

a die, said die being engaged with said substrate, said substrate comprising;

a first layer, wherein ball pads are dispersed throughout said first layer; and

a second layer including metal structures and an area proximate to a corner of the die, wherein a number of said ball pads of said first layer are associated with said area and wherein said metal structures of said second layer are routed away from said area.

2. A package as defined in claim 1, wherein said metal structures include signal traces.

3. A package as defined in claim 1, wherein said metal structures include voltage bus bars.

4. A package as defined in claim 1, wherein said area is defined as an area approximately two ball pitches away from the corner of the die.

5. A package as defined in claim 1, wherein said metal structures are not routed over said ball pads associated with said area.

6. A package as defined in claim 1, wherein said area is defined as an area approximately two ball pitches away from the corner of the die and wherein said metal structures are not routed over said ball pads associated with said area.

7. A method of forming a semiconductor package for a die including the steps of:

providing a substrate, said substrate having a first layer, wherein ball pads are dispersed throughout said first layer and a second layer having metal structures;

providing a die;

engaging said die with said substrate;

defining an area proximate a corner of the die, wherein a portion of said ball pads of said first layer are associated with said area; and

routing said metal structures of said second layer away from said area.

8. The method of claim 7, wherein the step of defining an area is performed by identifying an area two ball pitches away from a corner of the die.

9. The method of claim 7 wherein said step of routing said metal structures further includes routing said metal structures away from said ball pads associated with said area.

10. The method of claim 7, wherein the step of defining an area is performed by identifying an area two ball pitches away from a corner of the die and wherein the step of routing said metal structures further includes routing said metal structures away from said ball pads associated with said area.

11. The method of claim 7, wherein said metal structures of said second layer include signal traces.

12. The method of claim 7, wherein said metal structure of said second layer include voltage bus bars.

13. The method of claim 7 wherein said semiconductor package supports a range of die sizes.